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	Application No.	Applicant(s)
Notice of Allowability	10/742,896	HARANO ET AL.
	Examiner	Art Unit
	Laura M. Schillinger	2813
The MAILING DATE of this communication appears on the cover sheet with the correspondence address All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.		
1. X This communication is responsive to 12/23/03.		
2. 🔀 The allowed claim(s) is/are <u>1-5</u> .		
3. 🔀 The drawings filed on 23 December 2003 are accepted by the Examiner.		
4.		
<ul> <li>Attachment(s)</li> <li>1. ☑ Notice of References Cited (PTO-892)</li> <li>2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)</li> <li>3. ☑ Information Disclosure Statements (PTO-1449 or PTO/SB/0 Paper No./Mail Date 12/23/03</li> <li>4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material</li> </ul>	6. ☐ Interview Summary Paper No./Mail Dat 8), 7. ☑ Examiner's Amendr	te

## **DETAILED ACTION**

## **EXAMINER'S AMENDMENT**

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

Cancel claims 6-8.

Note: claims 1-5 were elected over the phone by Juan Marquez on 4/5/05; without traverse.

## Allowable Subject Matter

Claims 1-5 are allowed.

The following is an examiner's statement of reasons for allowance:.

In reference to claim 1, Yi ('481) teaches a display device comprising:

a thin film transistor substrate (11) which includes at least an insulation substrate having background layer on a surface thereof (13), a polysilicon layer formed over the background layer (15), gate electrodes (21) formed over the polysilicon layer by way of a first insulation layer (19) which covers the polysilicon layer(15), a second insulation layer covering the gate electrode (29), a pair of source/drain electrodes formed over the second insulation layer (23/25), the source/drain electrodes penetrating the second insulation layer and the first insulation layer and

Art Unit: 2813

being in contact with the polysilicon layer (15), and a third insulation layer (35) covering the wherein source/drain electrodes (23/25) (Fig.1),

and a barrier layer (130)made of molybdenum or molybdenum alloy which is formed below the conductive layer (121) and is in contact with the polysilicon layer (127/128) (Fig. 5d);

However Yi et al fails to teach the source/drain electrode includes a cap layer made of molybdenum or a molybdenum alloy which is formed over a conducive layer made of aluminum or an aluminum alloy and is in contact with the third insulation layer, and the source/drain electrode further includes a molybdenum oxide nitride film on a surface of the barrier layer which is contact with the conductive layer.

However, Meguro et al ('985) teaches the source/drain electrode (12) includes a cap layer made of molybdenum or a molybdenum alloy (22) which is formed over a conductive layer made of aluminum or an aluminum alloy (12- Col.4, lines: 50-60) and is in contact with the third insulation layer (8B) (Fig.1).

Yet even in combination, Yi and Meguro still fail to teach nor suggest Applicant's additional claimed limitation of the source/drain electrode further includes a molybdenum oxide nitride film on a surface of the barrier layer which is contact with the conductive layer.

Art Unit: 2813

Consequently, Applicant's claim language is not anticipated by prior art and claim 1 is deemed to contain allowable subject matter as explained above. Claims 2-5, act only to further narrow independent claim 1 and are therefore also deemed to be allowable over prior art.

## Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Laura M. Schillinger whose telephone number is (571) 272-1697. The examiner can normally be reached on M-T, R-F 7:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Laura Myblery

Laura M Schillinger Primary Examiner Art Unit 2813

4/15/05